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Compiling Your Design

... vhd" analyze -format **vhdI** MOD10 + ".vhd" analyze -format **vhdI** TOP + ".vhd ... Call the

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Creating Timing Specifications

... analyze -f vhdl file1.vhd analyze -f vhdl file2.vhd set_false_path...
write_script > "top.dc" sh dc2ncf "top.dc" exit. ...
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Compiling a Synopsys CPLD Design

... To derive a logical design, based on your VHDL/HDL description, enter the following Synopsys command: ... Enter the dc2ncf command at the Unix prompt as follows: ... www.xtra.xilinx.com/docsan/data/ alliance/syn/syn3_1.htm - 10k - Cached - Similar pages

Design Example

... Step 11 - Elaborate Your Design. To build the design based on your analyzed VHDL file, entering the following Synopsys command: elaborate scan. ... dc2ncf scan.dc. ... www.xtra.xilinx.com/docsan/data/ alliance/syn/syn1_6.htm - 29k - Cached - Similar pages

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rt.cs.tu-berlin.de/lehre/aes/flasher.script

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... Einlesen der Designfiles, Überprüfen der Abhängigkeiten analyze -format vhdl TOP
+ ".vhd ... output TOP + ".db" write_script > TOP + ".dc" sh dc2ncf TOP + ".dc" ...
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Introduction to Synopsys to XACT M1 Toolset

... Run the DC2NCF program to translate any constraints you have placed on the design in ... we will create a new design directory but copy the same VHDL source files ... www.ee.qub.ac.uk/dsp/support/documentation/ synopsys_to_xact/intro_synopsys_xact.html - 16k - Cached - Similar pages

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Implementation Of Fuzzy Controllers - Lago, Hinojosa, Jiménez, Barriga.. (1997) (Correct) according to a specific architecture based on a VHDL cell library. In both alternatives, the synthesis Fpga Implementation Of Fuzzy Controllers E. Lago, M. A. is accelerated by means of CAD tools which translate a high level description of the controller. A www.imse.cnm.es/online/1997/DCIS97.ELG.ps.gz

Signal Processing Applications using VHDL on Splash 2 - Sea Choi (1994) (Correct) Signal Processing Applications using VHDL on Splash 2 Sea H. Choi, Nalini K. Ratha, Moon J. change the design. Field Programmable Gate Arrays (FPGAs) have gained considerable attention recently to be functionally correct by simulation, it is translated into a Xilinx net list form. The net list is ftp.cps.msu.edu/pub/prip/ratha/viuf.ps.gz

Efficient Prototyping System Based on Incremental Design and.. - Yongjoo Kim (1995) (Correct) Cpu Sbus Sbus Interface Device Driver Custom Board Vhdl Simulator (proto, Part.Fpgas (sim. Part.Sim. which consists of a general-purpose CPU and a FPGA-based custom board. Using our prototyping poppy.snu.ac.kr/papers/ISCAS95.ps

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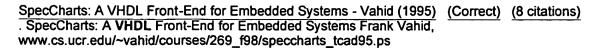
Rapid Architectural Design and Validation Using Program - Driven .. - Andrew Chien (1996) (Correct) signal assignment statement, in a language such as VHDL, can potentially generate an event, therefore, the A "back End. Compilation Synthesis Mapping VhdI Fpga Netlist Linked Executable Compiled Simulator www.ics.uci.edu/~dasdan/mypapers/dasdan-hldvt97.ps.gz

Standard Verilog-VHDL Interoperability - Victor Berman (Correct) Standard Verilog-VHDL Interoperability Victor Berman Cadence Design www.vhdl.org/vi/libutil/vhdl_verilog/interop.ps

A Versatile Design Validation Environment by Means of Software .. - Axel Jantsch (1994) (Correct) The hardware is simulated with the Synopsys VHDL simulator and the software is represented as C . A prototype board with two Xilinx XC4005 FPGAs and a local memory are connected to the system www.ele.kth.se/ESD/doc/ar94/axel/sims94.ps.gz

An EPLD Based Transient Recorder for Simulation of Video.. - Larsson University (Correct) Simulation of Video Signal Processing Devices in a VHDL Environment Close to System Level Conditions L. Hold/load 0 1 8 Reg 8 Fig. 3. Video Shifter Fpga Epld (fig. 4)In Replay Mode (play) Data Is Read tech-www.informatik.uni-hamburg.de/Personal/larsson/papers/epldtran springer Incs1142.ps.gz

The VHDL Standard - Meersman (1994) (Correct) Fax: 32(9)220.31.91 email: cme@e2s.be The VHDL Standard An overview of activities, organizations www.vlsivie.tuwien.ac.at/mike/VHDLReport.ps



The Virtual Wires Emulation System: A Gate-Efficient ASIC.. - Russell Tessier (1994) (Correct) (12 citations) for Computer Science Cambridge, MA 02139 Abstract FPGA-based ASIC development systems have become Emulation System includes a number of tools to **translate** a design into a group of interconnected FPGA netlists. Each logic partition is subsequently **translated** into gates in the target FPGA technology and ftp.cag.lcs.mit.edu/virtual_wires/fpga94.ps.Z

Sassy: A Language and Optimizing Compiler for Image.. - Hammes, Draper, Böhm (1999) (Correct) in hardware description languages such as VHDL. Sassy was developed as part of the Cameron systems consist of field-programmable gate arrays (FPGAs)memories and interconnection hardware, and can www.cs.colostate.edu/~draper/papers/hammes icvs99.ps

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be used to translate the XFL specification into a VHDL description capable of being implemented as a
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synthesis tool, called xfvhdl, can be used to translate the XFL specification into a VHDL description
www.imse.cnm.es/online/1998/ICECS98.ABB.ps.gz

A Front-End VHDL Editor for Synthesis tools. - Bouguerba Benzakki (Correct)
A Front-End VHDL Editor for Synthesis tools. T. Bouguerba, J. babar.inria.fr/pub/croap/General/VIUF_San-Diego.ps

A FPGA based Forth microprocessor - Leong Tsang (Correct)
board. The MSL16 design was synthesised from a VHDL description using the Synopsys Inc. FPGA
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Mesh Routing Topologies For FPGA Arrays - Scott Hauck (1994) (Correct) (3 citations) February 1994. Mesh Routing Topologies For FPGA Arrays Scott Hauck, Gaetano Borriello, Carl www.ece.nwu.edu/~hauck/publications/RoutingTop.ps

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